

M-15281US
10/753,673REMARKS

Applicants have noted in the specification that the inventive source/drain adjust they disclose is not the same as halo implant. For example, on page 6, lines 11 – 20, Applicants noted that a halo implant surrounds both the drain and source of the affected transistor. As known in the art, halo implants act to limit lateral diffusion of the source and drain regions. In that regard, consider Figure 1 and 3 of the specification: the adjust implant 85 only underlies source/drain 48 and source drain 22, respectively. In other words, for any given transistor, there is no adjust implant that underlies both its source and drain. This is important because (by not underlying both the source and drain for either the select or floating gate transistor) the channel doping for either transistor is not affected. Thus, “n region 85 provides the benefits of decreased programming voltage and better punch-through resistance without disadvantageously affecting threshold voltages.”

To better highlight the inventive nature of their source/drain adjust implant as compared to a conventional halo implant, claim 1 has been amended to recite “an N implant underlying only the P+ diffusion region that forms the floating gate transistor’s drain such that an N implant does not underlie either of the P+ diffusion regions forming the select gate’ transistor drain and the floating gate’s transistor’s source.” As discussed above, such an amendment is fully supported by the specification and thereby introduces no new matter.

The cited prior art stands in sharp contrast. In particular, the Kang reference (U.S. 6,180,443) cited to provide the teaching of an n implant merely discloses conventional halo implants (Col. 5, lines 13-15 expressly denotes regions 30 in Figure 5 as “halo” regions). Because these are halo regions, they underlie both the source and the drain for both NMOS transistors shown in Figure 5. Thus, Kang makes absolutely no teaching or suggestion for the

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inventive source/drain adjust implant of Figure 3 that underlies only the shared source/drain region between the floating gate and select gate transistors as recited in claim 1.

The remaining cited prior art provides nothing further. Thus, claim 1 and its dependent claims 2 through 9 are allowable over the cited prior art.

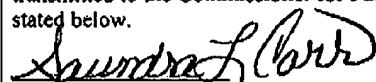
Applicants have provided formal drawings as requested by the Examiner.

Accordingly, Applicants respectfully submit that Claims 1-9 are in proper form for allowance. Reconsideration and withdrawal of the rejections are respectfully requested and a timely Notice of Allowance is solicited.

If there are any questions regarding any aspect of the application, please call the undersigned at (949) 752-7040.

Certificate of Transmission

I hereby certify that this correspondence is being facsimile transmitted to the Commissioner for Patents on the date stated below.


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Dated: July 25, 2005

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Respectfully submitted,



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